REMARKS/ARGUMENTS

Claims 1-11 are pending.

Claims 5-10 are allowed.

Claims 1-3 and 11 are rejected.

Claim 4 is objected to.

The Applicants wish to thank the Examiner for allowing claims 5-10 and for indicating that claim 4 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In view of the following remarks, the Applicants request favorable reconsideration and allowance of the present application.

The rejection of claims 1-3 and 11 under 35 U.S.C. §103(a) as being unpatentable over "Block-Level Fault Isolation Using Partition Theory and Logic Minimization Techniques" by C.J. Richard Shi ("Shi") in view of U.S. Patent No. 6,536,024 ("Hathaway") and Applicants' traversal thereof

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The present invention relates to the use of clock gating or signal gating during testing of an electronic device. The results of the testing may be used to localize defects existing in the device to one or more segments on the device. (Page 3, lines 6-10). Further, "FIG. 1 is a schematic block diagram of a computer system chip in which clock gating is employed" and "FIG. 4 is a block diagram showing another chip arrangement in which clock gating is employed." (Page 2, lines 20-21; page 3, lines 1-2).

The article by Shi describes an approach "to localize a failure within a chip boundary as rapidly as possible in order to expedite the rework process and to minimize its overall impact on manufacturing throughput and cycle time." (Shi, page 319, col. 1,

lines 3-7). The rework process may include repairing or replacing. (Shi, page 319, col. 1, lines 26-31). The article by Shi describes formulas and theories to isolate or locate faults to an individual circuit block, which is the smallest replaceable unit. (Page 321, col. 2, lines 2-3).

The Hathaway patent describes a "method for synthesizing a logic circuit that is driven by a clock signal, and that has a plurality of clock domains each having a plurality of clock sinks..." (Hathaway, col. 4, lines 9-11). The Hathaway patent appears to attempt to reduce the power consumption of integrated circuits. (col. 3, line 65 - col. 4, line 5) More specifically, the Hathaway patent provides a clock gating method for improving the clock gating efficiency of low power clock signal distribution networks. The above method may be used in a microprocessor design that provides reduced power consumption. (Hathaway, col. 25, lines 23-29).

To reject independent claims 1, 2 and 11 as unpatentable, the Office Action states that the Shi article teaches "a test control device adapted to couple to an electronic device . . . and control the electronic device to identify one of the segments that is a source of a failure by selectively disabling at least one of the segments (Claims 1-3 and 11:see page 319, col. 1, paragraph 2, lines 8-13)." (Office Action, page 2, line 23 to page 3, line 2). The Applicants respectfully disagree. The portion of the article by Shi cited in the Office Action is merely a statement of a problem of locating faulty dice and performing a repair or replace on them. The article by Shi does not appear to indicate specifically how the faulty dice are located. More specifically, the article by Shi does not appear to disclose, teach, or suggest identifying one of the segments [of a device] that is a source of a failure by selectively disabling at least one of the segments, and consequently does not appear to disclose, teach or suggest a test control device

adapted to control an electronic device to perform such a step, as required by claims 1, 2 and 11.

Applicants agree that "Shi does note [sic] teach a method [of] using clock gating or signal gating." (Office Action, page 3, line 3). To reject independent claims 1, 2 and 11 as unpatentable over the Shi article in view of the Hathaway patent, the Office Action states, "It would have been obvious to the person having ordinary skill in the art at the time the invention was made to modify Shi to use clock gating, as taught by Hathaway . . ." (Office Action, page 3, 5-7). The Applicants respectfully disagree. For the reasons described above, the Office Action's proposition that the Shi article teaches certain aspects of the present invention does not appear to be supported by the Shi article; and the Hathaway patent does not overcome these deficiencies. Additionally, the claimed invention and U.S. Patent No. 6,536,024 (Hathaway) were, at the time the invention of this application was made, owned by (or subject to a duty of assignment to) International Business Machines Corporation, the assignee of this application. It is noted that U.S. Patent No. 6,536,024 appears to qualify as prior art relative to this application, if at all, only under subsection (e) of 35 USC §102. Accordingly, pursuant to 35 USC §103(c), U.S. Patent No. 6,536,024 is disqualified from being used in a rejection under 35 USC §103 against the claims of this application. (See MPEP Sec. 706.02(l)(2)).

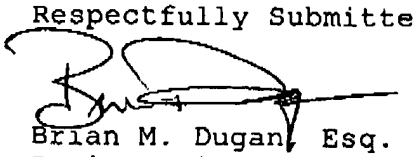
Alternatively, if the Hathaway patent were prior art, the Applicants respectfully disagree with the rejection of independent claims 1, 2 and 11 as unpatentable based thereon. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. MPEP §2143.01. Although, the Hathaway patent describes the use of clock gating in an integrated circuit (IC) design, the goal of

the Hathaway patent is to reduce power consumption by improving clock gating efficiency (Hathaway, col. 9, lines 59-64; col. 25 lines 23-28). The Hathaway patent does not appear to be concerned with or describe testing an IC to localize any defects in the IC to one or more segments of the IC. Consequently, there appears to be no basis in the art for combining the teachings of the Shi article with the Hathaway patent.

For the above reasons, the Applicants submit that independent claims 1, 2 and 11 are patentable over the article by Shi in view of the Hathaway patent, and respectfully request that claims 1, 2 and 11 and claim 3, which depends therefrom, be allowed. All of the claims are believed to be in condition for allowance and passage to issue is respectfully solicited.

Applicants do not believe any fees are due regarding this Response. If any fees are required, however, please charge Deposit Account No. 04-1696. Applicants encourage the Examiner to telephone Applicants' attorney to discuss the response should any issues remain.

Respectfully Submitted,



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